PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-357735
(43)Date of publication of application : 26.12.2000

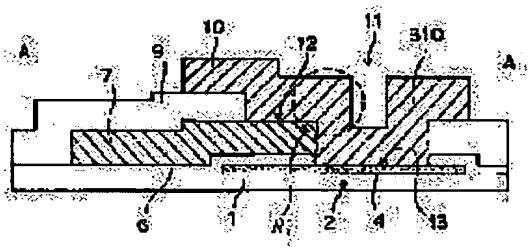
(51)Int.CI. H01L 21/768
G02F 1/1365
G09F 9/30
H01L 21/28
H01L 29/786
H01L 21/336
H01L 29/861

(21)Application number : 11-166945
(22)Date of filing : 14.06.1999

(71)Applicant : SEIKO EPSON CORP
(72)Inventor : KITAWADA KIYOBUMI
KIMURA MUTSUMI
MAEDA HIROSHI

(54) SEMICONDUCTOR DEVICE, ELECTRO-OPTICAL DEVICE AND MANUFACTURE OF THE SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the number of contact holes required for conduction with the source region or the drain region of a semiconductor layer, and to realize closest packed arrangement.
SOLUTION: Since a gate electrode 7, a source region 4 of a semiconductor layer 2 and a wiring 10 are constituted, so that a conduction part 310 integrally conduct them via one contact hole 11 passing through an interlayer insulating film 9 and a gate insulating film 6, the number of contact holes 11 required for conduction with the source region 4 of the semiconductor layer 2 is made to be one and closest packed arrangement is realized.



LEGAL STATUS

[Date of request for examination] 09.06.2003
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision

of rejection]
[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] A semi-conductor layer and the 1st insulator layer formed so that said semi-conductor layer top might be covered, The 1st wiring formed on said 1st insulator layer, and the 2nd insulator layer formed on said 1st insulator layer so that said 1st wiring might be covered, The semiconductor device characterized by providing the flow section which flows through the 2nd wiring formed on said 2nd insulator layer, and the source field or the drain field, said 1st wiring and said wiring of the 2nd of said semi-conductor layer through one contact hole which penetrates said 1st and 2nd insulator layers.
[Claim 2] The semiconductor device according to claim 1 characterized by forming said the 2nd wiring and said flow section in one.
[Claim 3] The semiconductor device according to claim 1 or 2 characterized by said flow section having a connection side with the top face of said 1st wiring.
[Claim 4] It is a semiconductor device given in any 1 term among claim 1 to claims 3 characterized by said flow section having a connection side with the top face of the source field of said semi-conductor layer, or a drain field.
[Claim 5] It is a semiconductor device given in any 1 term among claim 1 to claims 4 characterized by having the gate electrode with which said 1st wiring intersects the channel field of said semi-conductor layer.
[Claim 6] Two or more data lines installed in the direction which crosses to the installation direction of two or more scanning lines and this scanning line on the substrate, It has the pixel field formed in the shape of a matrix by two or more common feeders arranged in parallel in this data line, and said data line and said scanning line. To each of this pixel field The 1st thin film transistor by which a scan signal is supplied to the 1st gate electrode through said scanning line, The 2nd thin film transistor by which the picture signal supplied from said data line through this 1st thin film transistor is supplied to the 2nd gate electrode, In between layers with the counterelectrode corresponding to said two or more pixel electrodes ranging over the pixel electrode formed for said every pixel field, said scanning line, and said data line It is the electro-optic device which has a light emitting device possessing the luminous layer which emits light according to the drive current which flows between said pixel electrodes and said counterelectrodes when said pixel electrode connects with said common feeder electrically through said 2nd thin-film transistor. The gate dielectric film formed so that the semi-conductor layer top of said 1st thin film transistor might be covered, Said 2nd gate electrode formed on said gate dielectric film, and the 1st flowing wiring, The interlayer insulation film formed on said gate dielectric film so that said 1st wiring might be covered, The 2nd wiring formed on said interlayer insulation film, The electro-optic device characterized by providing the flow section which flows through the source field or the drain field, said 1st wiring, and said wiring of the 2nd of said semi-conductor layer through one contact hole which penetrates said gate dielectric film and said interlayer insulation film.
[Claim 7] The process which forms a semi-conductor layer, and the process which forms the 1st insulator layer so that said semi-conductor layer top may be covered, The process which forms the 1st wiring on said 1st insulator layer, and the process which forms the 2nd insulator layer on said 1st insulator layer so that said 1st wiring may be covered, The process which forms a contact hole so that said 1st and 2nd insulator layers may be penetrated and the source field of said semi-conductor layer or a drain field, and said 1st wiring may be exposed, The characterizing [it]-by providing process which forms the 2nd wiring which flows in said flow section while forming the flow section in said contact hole on insulator layer said 2nd [the] manufacture approach.
[Claim 8] The manufacture approach of the semiconductor device according to claim 7 characterized by forming said contact hole of dry etching.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention belongs to the technical field of the manufacture approach of of the electro-optic device and semiconductor device which carry the semiconductor device used for the drive circuit of a semiconductor device or liquid crystal equipment, the switching means of EL (electroluminescence) component, etc., an EL element, etc. Especially this invention relates to the manufacture approach of the semiconductor device constituted so that it might flow through a semi-conductor layer and two wiring formed on it in one through one contact hole, an electro-optic device, and a semiconductor device.
[0002]
[Description of the Prior Art] Generally, when it constitutes diode using a thin film transistor (TFT is called hereafter.) as a semiconductor device, as shown in drawing 11 , the gate electrode 102 and the source field 103 of a thin film transistor 101 are short-circuited, and it constitutes. In this case, if TFT is n mold, the drain field 104 side will serve as [the source field 103 side] cathode in an anode plate.
[0003] The general structure of such a thin film transistor 101 is shown in drawing 12 and drawing 13 . Here, the top view in which drawing 12 shows the general structure of a thin film transistor 101, and drawing 13 are the A-A sectional views of drawing 12 .
[0004] As shown in these drawings, the semi-conductor layer 106 is formed on the substrate 105.
[0005] Gate dielectric film 107 is formed on this semi-conductor layer 106, and the gate electrode 108 is formed so that channel field 106a of the semi-conductor layer 106 may be intersected through this gate dielectric film 107. The end of the gate electrode 108 is installed and the tip is connected with the source wiring 110 formed on the interlayer insulation film 109 through the 1st contact hole 111 which penetrates an interlayer insulation film 109. This source wiring 110 is installed towards the source field 103 of the semi-conductor layer 106, and is connected with the source field 103 of the semi-conductor layer 106 through the 2nd contact hole 112 where that tip penetrates an interlayer insulation film 109 and gate dielectric film 107. In addition, the drain field 104 of the semi-conductor layer 106 is connected to wiring which omitted illustration through the 3rd contact hole 113.
[0006]
[Problem(s) to be Solved by the Invention] However, in the thin film transistor 101 constituted as mentioned above, since it is necessary to form two contact holes 111 and 112 in order to make it flow through the gate field 102 and the source field 103, and it is moreover necessary to arrange with allowances in each contact holes 111 and 112 in consideration of the alignment gap in these contact holes 111 and 112 to some extent, the technical problem that it becomes a failure for carrying out closest packing arrangement occurs.
[0007] This invention is made based on this technical problem, the number of contact holes required since it flows with the source field of a semi-conductor layer or a drain field is reduced, and it aims at offering the manufacture approach of the semiconductor device which can carry out closest packing arrangement, an electro-optic device, and a semiconductor device.
[0008]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the semiconductor device of this invention A semi-conductor layer and the 1st insulator layer formed so that said semi-conductor layer top might be covered, The 1st wiring formed on said 1st insulator layer, and the 2nd insulator layer formed on said 1st insulator layer so that said 1st wiring might be covered, It is characterized by providing the flow section which flows through the 2nd wiring formed on said 2nd insulator layer, and the source field or the drain field, said 1st wiring and said wiring of the 2nd of said semi-conductor layer through one contact hole which penetrates said 1st and 2nd insulator layers.

0009] Since according to the configuration which this invention requires it constituted so that it might flow through the ource field or the drain field, the 1st wiring, and wiring of the 2nd of a semi-conductor layer in one by one contact hole vhich penetrates the 1st and 2nd insulator layers, there is flume ****** which the number of contact holes required ince it flows with the source field of a semi-conductor layer or a drain field is set to one, and can carry out closest ›acking arrangement.
0010] According to the mode of 1 of this invention, said the 2nd wiring and said flow section are characterized by ›eing formed in one. According to this configuration, since the flow section is formed in one with the 2nd wiring, it is :ffective in the ability to reduce the man day for forming the flow section.
0011] According to the mode of 1 of this invention, it is characterized by said flow section having a connection side vith the top face of said 1st wiring. According to this configuration, since the flow section is connected to the 1st wiring ınd flat-surface target, connection between these can be ensured. Therefore, it is effective in becoming possible to ›ecome unnecessary to take an alignment gap of a contact hole into consideration so much, and to carry out further :losest packing arrangement by this.
0012] the voice of 1 of this invention -- if it depends like, it will be characterized by said flow section having a :onnection side with the top face of the source field of said semi-conductor layer, or a drain field. According to this :onfiguration, since the flow section is connected to the source field or drain field, and flat-surface target of a semi-:onductor layer, connection between these can be ensured. Therefore, it is effective in becoming possible to become ınnecessary to take an alignment gap of a contact hole into consideration so much, and to carry out further closest ›acking arrangement also by this.
0013] According to the mode of 1 of this invention, said 1st wiring is characterized by having the gate electrode which intersects the channel field of said semi-conductor layer. According to this configuration, when TFT constitutes diode, for example, there is flume ****** which can carry out closest packing arrangement.
[0014] Two or more data lines with which the electro-optic device of this invention was installed in the direction which crosses to the installation direction of two or more scanning lines and this scanning line on the substrate, It has the pixel field formed in the shape of a matrix by two or more common feeders arranged in parallel in this data line, and said data line and said scanning line. To each of this pixel field The 1st thin film transistor by which a scan signal is supplied to the 1st gate electrode through said scanning line, The 2nd thin film transistor by which the picture signal supplied from said data line through this 1st thin film transistor is supplied to the 2nd gate electrode, In between layers with the counterelectrode corresponding to said two or more pixel electrodes ranging over the pixel electrode formed for said every pixel field, said scanning line, and said data line It is the electro-optic device which has a light emitting device possessing the organic-semiconductor film which emits light according to the drive current which flows between said pixel electrodes and said counterelectrodes when said pixel electrode connects with said common feeder electrically through said 2nd thin-film transistor. The gate dielectric film formed so that the semi-conductor layer top of said 1st thin film transistor might be covered, Said 2nd gate electrode formed on said gate dielectric film, and the 1st flowing wiring, The interlayer insulation film formed on said gate dielectric film so that said 1st wiring might be covered, It is characterized by providing the flow section which flows through the 2nd wiring formed on said interlayer insulation film, and the source field or the drain field, said 1st wiring and said wiring of the 2nd of said semi-conductor layer through one contact hole which penetrates said gate dielectric film and said interlayer insulation film.
[0015] Since two TFT(s) are needed as a switching element for every pixel in the electro-optic device constituted as mentioned above, compared with the liquid crystal equipment which can be constituted from one TFT, a pixel field becomes narrow for every pixel. Then, since it constituted from this invention so that it might flow through the source field or the drain field, the 1st wiring, and wiring to the 2nd of the 1st of the semi-conductor layer of a semiconductor device in one by one contact hole which penetrates gate dielectric film and an interlayer insulation film in the electro-optic device of this configuration ** which the number of contact holes required since it flows with the source field of the semi-conductor layer of the 1st semiconductor device or a drain field is set to one, and can carry out closest packing arrangement Therefore, it becomes possible to extend a pixel field.
[0016] The process in which the manufacture approach of the semiconductor device of this invention forms a semi-conductor layer, and the process which forms the 1st insulator layer so that said semi-conductor layer top may be covered, The process which forms the 1st wiring on said 1st insulator layer, and the process which forms the 2nd insulator layer on said 1st insulator layer so that said 1st wiring may be covered, The process which forms a contact hole so that said 1st and 2nd insulator layers may be penetrated and the source field of said semi-conductor layer or a drain field, and said 1st wiring may be exposed, While forming the flow section in said contact hole, it is characterized by providing the process which forms the 2nd wiring which flows in said flow section on an insulator layer said 2nd [the].

[0017] According to the configuration which this invention requires, a contact hole is formed so that the source field of a semi-conductor layer or a drain field, and the 1st wiring may be exposed. Since the 2nd wiring which flows in the flow section was formed on the insulator layer the 2nd while forming the flow section in the contact hole There is flume ****** which can manufacture the semiconductor device with which the number of contact holes required since it flows with the source field of a semi-conductor layer or a drain field was set to one, and closest packing arrangement was carried out.
[0018] According to the gestalt of 1 of this invention, it is characterized by forming said contact hole of dry etching. According to this configuration, since the contact hole was formed by dry etching, it is effective in that what a contact hole runs through a semi-conductor layer, and is formed is lost, and connect superficially and the source field or drain field of a contact hole and a semi-conductor layer can ensure these connection.
[0019]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained based on a drawing.
[0020] (Structure of a semiconductor device) As a semiconductor device which drawing 1 requires for 1 operation gestalt of this invention, the top view of TFT and drawing 2 are the A-A sectional views of TFT shown in drawing 1 . In addition, TFT concerning this operation gestalt applies this invention to the circuit shown in drawing 11 .
[0021] As shown in these drawings, on the substrate 1 which consists of a-Si film, the semi-conductor layer 2 which consists of p-Si is formed. In this semi-conductor layer 2, the source field 4 and the drain field 5 are established in the both sides of the channel field 3.
[0022] Gate dielectric film 6 is formed on this semi-conductor layer 2, and the gate electrode 7 is formed so that the channel field 3 of the semi-conductor layer 2 may be intersected through this gate dielectric film 6. The end of this gate electrode 7 is installed and is installed to the location which makes a U-turn further and laps with the source field 4 of the semi-conductor layer 2.
[0023] Moreover, on gate dielectric film 6, the interlayer insulation film 9 is formed so that the gate electrode 7 may be covered, and wiring 10 is formed on this interlayer insulation film 9. This wiring 10 is installed to the location with which the gate electrode 7 and the source field 4 of the semi-conductor layer 2 lap as mentioned above.
[0024] And the gate electrode 7, the source field 4 of the semi-conductor layer 2, and wiring 10 lap through gate dielectric film, in the contact hole 11 which penetrated an interlayer insulation film 9 and gate dielectric film 6, the flow section 310 is formed and this flow section is prepared in one with wiring 10. Thus, since wiring 10 and the flow section 310 are formed in one in one contact hole 11, the man day for forming the flow section 310 in a contact hole can be reduced.
[0025] This contact hole 11 has the connection side 12 with the up flat surface (top face) of the gate electrode 7, and has the connection side 13 with the up flat surface of the source field 4 of the semi-conductor layer 2 further. Thus, since the source field 4 of a contact hole 11, the gate electrode 7, and the semi-conductor layer 2 has the part which has connected superficially, more certainly electric connection can be made. For that purpose, as an area of the connection side 12, two or more [4-micrometer] are desirable, and two or more [4-micrometer] are desirable as an area of the connection side 13, for example.
[0026] In addition, the drain electrode 5 of the semi-conductor layer 2 is connected to wiring which omitted illustration through the contact hole 14.
[0027] Thus, ** which the number of the contact holes 11 required since it constituted so that the flow section 310 might flow through the gate electrode 7, the source field 4 of the semi-conductor layer 2, and wiring 10 in one in this operation gestalt through the contact hole 11 which penetrates an interlayer insulation film 9 and gate dielectric film 6, and it flows with the source field 4 of the semi-conductor layer 2 is set to one, and can carry out closest packing arrangement
[0028] Moreover, it is desirable at the point which connection of the gate electrode 7 and wiring 10 is obtained with the pass of R2 shown in drawing 1 even when an open circuit arises in the part of R1 by the side of wiring 10 in the structure shown in drawing 2 , and serves as positive connection.
[0029] In addition, although it had flowed through the source field 4 of the semi-conductor layer 2 in one with the gate electrode 7 and wiring 10 through the contact hole 11, you may constitute from this operation gestalt so that it may flow in one with a gate electrode and wiring by one contact hole also about the gate field of a semi-conductor layer.
[0030] (The manufacture approach of a semiconductor device) Next, the manufacture approach of TFT shown in drawing 1 and drawing 2 is explained.
[0031] It is drawing for drawing 5 to explain the production process of TFT concerning this operation gestalt from drawing 3 .
[0032] As first shown in drawing 3 (a), by irradiating excimer laser light, such as KrF or XeCl, two times 300 to 600

nJ/cm on the substrate 1 which consists of a-Si film, the a-Si film is crystallized and the p-Si film 301 with a thickness of 20nm - 100nm is obtained.
[0033] Next, as shown in drawing 3 (b), the photoresist mask 302 of the configuration equivalent to the semi-conductor layer 2 is formed on the p-Si film 301 through resist spreading, exposure processing, and a development.
[0034] Next, as shown in drawing 3 (c), by using the photoresist mask 302 as a mask, using chlorine-based gas, it etches and the p-Si layer 303 of the configuration equivalent to the semi-conductor layer 2 is formed for the p-Si film 301 by RIE (reactive ion etching). In addition, the wet etching using a drug solution, such as using and etching ****** in addition to dry etching like RIE, can also be used.
[0035] next, it is shown in drawing 3 (d) -- as -- PECVD after exfoliating the photoresist mask 302 -- the gate dielectric film 6 of 50-120nm thickness is formed by law by making TEOS (tetraethyl orthochromatic silicate) and oxygen gas into material gas. Here, SiH4 and oxygen gas may be used as material gas.
[0036] Next, TOREJISUTOMASUKU 304 is formed in the location equivalent to the channel field 3 of the semi-conductor layer 2 on the p-Si layer 303 as shown in drawing 3 (e). And this photoresist mask 304 is used as a mask, with ion-implantation, 1x1013 to 2x1014 phosphorus ion /is injected into the p-Si layer 303 with the dose of 2 cm as for example, impurity ion, and the source field 4 and the drain field 5 are formed.
[0037] next, the gate-dielectric-film 6 top as shown in drawing 4 (f), after removing the photoresist mask 304 -- PVD (physical vapour deposition) -- the 500nm aluminum film 305 is formed by law 200-600nm thickness and here.
[0038] Next, as shown in drawing 4 (g), the photoresist mask 306 of the configuration equivalent to the gate electrode 7 is formed. And the gate electrode 7 as exfoliates and shows the photoresistor pattern 306 to drawing 4 (h) is formed after etching the aluminum film 305 by the RIE method by using the photoresist mask 306 as a mask using a fluorine system or chlorine-based gas.
[0039] next, it is shown in drawing 4 (i) -- as -- the gate electrode 7 -- a wrap -- like -- TEOS and oxygen gas -- material gas -- carrying out -- PECVD -- the interlayer insulation film 9 with a thickness of 1200nm is formed by law 300-1500nm and here.
[0040] Next, as shown in drawing 4 (j), the photoresist mask 307 by which patterning was carried out to the configuration equivalent to a contact hole 11 is formed.
[0041] And as shown in drawing 5 (k), the contact hole 11 which penetrates an interlayer insulation film 9 and gate dielectric film 6 by using the photoresist mask 307 as a mask by the reactive-ion-etching method (the RIE method) using the fluorine system 5, for example, C2HF, and CHF3 is formed, and the photoresist mask 307 is exfoliated. Thus, by forming a contact hole 11 by dry etching, what a contact hole 11 runs through the semi-conductor layer 2, and is formed is lost.
[0042] next, it is shown in drawing 5 (l) -- as -- an interlayer insulation film 9 top -- PVD (physical vapour deposition) -- the aluminum film 308 of 300-1000nm thickness is formed by law.
[0043] Next, as shown in drawing 5 (m), the photoresist mask 309 of a configuration from which it was removed except the part equivalent to wiring 10 is formed on the aluminum film 308. The photoresist mask 309 is exfoliated after etching by the RIE method using chlorine-based gas in the aluminum film 308 by using the photoresist mask 309 as a mask. As shown in drawing 5 (n), while wiring 10 is formed by this, the flow section 310 through which it flows in this is formed in a contact hole 11.
[0044] According to this operation gestalt, it is possible to manufacture the semiconductor device with which the number of the contact holes 11 required since it flows through the source field of the semi-conductor layer 2 or a drain field, the gate electrode 7, and wiring 10 was set to one, and closest packing arrangement was carried out as mentioned above.
[0045] (1st operation gestalt of an electro-optic device) Next, the active-matrix mold display using the organic thin film EL element of a charge impregnation mold as 1st operation gestalt of the electro-optic device of this invention is explained.
[0046] Drawing 6 is the block diagram showing the configuration of such a active-matrix mold indicating equipment.
[0047] The pixel field 607 corresponding to the crossing of two or more data lines sig installed in the direction which crosses on the transparence substrate 600 to the installation direction of two or more scanning lines gate and this scanning line gate, two or more common feeders com and the data line sig which are arranged in parallel in this data line sig, and the scanning line gate consists of displays 601 shown in drawing 6 . To the data line sig, the shift register, the level shifter, the video line, and the data side drive circuit 603 equipped with an analog switch are constituted. To the scanning line, the scan side drive circuit 604 equipped with a shift register and a level shifter is constituted.
[0048] Moreover, 1st TFT620 by which a scan signal is supplied to each of the pixel field 607 through the scanning line at a gate electrode, The retention volume cap holding the picture signal supplied from the data line sig through this 1st

TFT620, When the picture signal held with this retention volume cap connects with the common feeder com electrically through 2nd TFT630 supplied to a gate electrode, and 2nd TFT630, the light emitting device 640 into which a drive current flows consists of common feeders com.

[0049] The A-A sectional view of drawing 7 and drawing 9 of the top view and drawing 8 which show the configuration of the pixel field 607 of the above [drawing 7] are the B-B sectional views of drawing 7 .

[0050] As shown in drawing 7 and drawing 8 , the 2nd semi-conductor layer 730 which constitutes the 1st semi-conductor layer 720 and 2nd TFT630 which constitute 1st TFT620 using two island-like semi-conductor film also in which pixel field is formed. The junction electrode 735 connected with the drain field of the 2nd semi-conductor layer 730 electrically through the KONTAKU hole 761 of the 1st interlayer insulation film 751, and the pixel electrode 741 has connected with this junction electrode 735 electrically through the KONTAKU hole 762 of the 2nd interlayer insulation film 752 to it. The laminating of the luminous layer 743 and Counterelectrode OP which consist of a hole-injection layer 742, an organic-semiconductor ingredient, etc. is carried out to the upper layer side of this pixel electrode 741. Here, Counterelectrode OP is formed over two or more pixel fields 607 ranging over the data line sig etc. The common feeder com has connected with the source field of the 2nd semi-conductor layer 730 electrically through a contact hole 763.

[0051] On the channel field of the 2nd semi-conductor layer 730, the gate electrode 731 is formed through gate dielectric film 750. Here, as shown in drawing 9 , this gate electrode 731 is installed even in the drain field of the 1st semi-conductor layer 720. Furthermore, on it, wiring 710 is formed through the 1st interlayer insulation film 751 formed on the gate electrode 731. Therefore, wiring 710 is arranged so that it may lap with the gate electrode 731, the drain field of the 1st semi-conductor layer 720, and flat-surface target which were installed.

[0052] And the contact hole 711 in which the 1st interlayer insulation film 751 and gate dielectric film 750 were penetrated, and the flow section 709 was formed is established in the location with which the installed gate electrode 731, the drain field of the 1st semi-conductor layer 720, and wiring 710 lap in one with wiring 710. This contact hole 711 has the connection side 712 with the up flat surface of the installed gate electrode 731, and has the connection side 713 with the up flat surface of the drain field of the 1st semi-conductor layer 720 further.

[0053] Moreover, the source field of the 1st semi-conductor layer 720 is electrically connected with the data line sig through the contact hole 764 which penetrates the 1st interlayer insulation film 751 and gate dielectric film 750. Furthermore, in the 1st semi-conductor layer 720, on the channel field, it is formed so that the gate electrode 721 projected from the scanning line gate through gate dielectric film 750 may intersect this channel field.

[0054] ** which can carry out closest packing arrangement as mentioned above since the number of contact holes required since it flows through the gate electrode 731 and wiring 710 which were installed with the drain field of the 1st semi-conductor layer 720 with this operation gestalt was set to one Therefore, it becomes possible to extend the pixel field 607, and area of a pixel electrode can be enlarged.

[0055] In wiring of this drawing 6 thru/or drawing 9 , and the display which has pixel structure, if a scan signal is supplied to the gate electrode 721 of 1st TFT620 through the scanning line gate, TFT620 is turned on, and through the data line sig, a picture signal will be supplied to the drain side concerned of TFT, and will be held at retention volume cap. And if the picture signal held at this retention volume is supplied to the gate electrode 731 of 2nd TFT630 and TFT630 is turned on, a drive current will be supplied from Feeder com side (source side of TFT630). This current is supplied to the drain side of TFT630, in a pixel, an electron hole is poured in through the hole-injection layer 742 from the pixel electrode 741, an electron is poured in from Counterelectrode op, and an electron hole and an electron recombine it by the luminous layer 743, and it produces luminescence.

[0056] (2nd operation gestalt of an electro-optic device) Next, the active-matrix mold display using the organic thin film EL element of the charge impregnation mold with which a gestalt differs from the above-mentioned electro-optic device as 2nd operation gestalt of the electro-optic device of this invention is explained.

[0057] Although the display concerning this operation gestalt is the same configuration as the display fundamentally shown in drawing 6 , the gestalten of each pixel field differ. However, with this operation gestalt, the two data lines sig are formed at a time, and a signal is supplied to the pixel field which adjoins along with these data lines sig, respectively from the different data line sig.

[0058] Drawing 10 is the top view showing the configuration of the pixel field 807 in the display concerning this operation gestalt.

[0059] as shown in drawing 10 , also in which pixel field 807, 1st TFT820 forms near the scanning line gate along with the scanning line gate -- having -- the pixel field 807 -- 2nd TFT830 is mostly formed in the center.

[0060] the drain field of the 2nd semi-conductor layer 930 which constitutes 2nd TFT830 -- the KONTAKU hole 961 of the 1st interlayer insulation film -- minding -- the 1st junction electrode 935 -- electric -- connecting -- this -- it has

;onnected with the 1st junction electrode 935 electrically through the KONTAKU hole 962 of the 2nd interlayer nsulation film at the 2nd junction electrode 936. The 2nd junction electrode 936 has branched on both sides along with he data line sig from near the center of the pixel field 807, and is electrically connected to each circular pixel electrode)41 and 942 which carried out the pixel field 807 for 2 minutes and which has been mostly arranged in the center.
0061] The laminating of a hole-injection layer, the organic-semiconductor film, and the counterelectrode is carried out o the upper layer side of this pixel electrode 941. Here, the counterelectrode is formed over two or more pixel fields 307 ranging over the data line sig etc. The common feeder com has connected with the source field of the 2nd semi-;onductor layer 930 electrically through a contact hole 963.
'0062] On the channel field of the 2nd semi-conductor layer 930, the gate electrode 931 is formed through gate lielectric film. The gate electrode 931 is installed in the bottom of the common feeder com, and the retention volume ;ection 990 to 2nd TFT830 by the gate electrode 931 and the common feeder com countering by this is formed.
'0063] Furthermore, this gate electrode 931 is installed even in the drain field of the 1st semi-conductor layer 920 which ;onstitutes 1st TFT820. Furthermore, on it, wiring 910 is formed through the 1st interlayer insulation film formed on the gate electrode 931. Therefore, wiring 910 is arranged so that it may lap with the gate electrode 931, the drain field of the 1st semi-conductor layer 920, and flat-surface target which were installed.
'0064] And the contact hole 911 in which the flow section which penetrates the 1st interlayer insulation film and gate lielectric film was formed is established in the location with which the installed gate electrode 931, the drain field of the 1st semi-conductor layer 920, and wiring 910 lap in one with wiring 910. About such structure, it is the same as that of what was shown in drawing 9 .
[0065] Moreover, the source field of the 1st semi-conductor layer 920 is electrically connected with the data line sig through the contact hole 964 which penetrates the 1st interlayer insulation film and gate dielectric film. Furthermore, in the 1st semi-conductor layer 920, on the channel field, it is formed so that three gate electrodes 921 projected from the scanning line gate through gate dielectric film may intersect this channel field.
[0066] ** which can carry out closest packing arrangement since the number of contact holes required since it flows through the drain field of the 1st semi-conductor layer 920, the installed gate electrode 931, and wiring 910 also in this operation gestalt was set to one Therefore, it becomes possible to extend the pixel field 807, and area of a pixel electrode can be enlarged.
[0067] With the above-mentioned operation gestalt, although explained using TFT, also in the structure which forms a transistor, it is applicable not only to this but a silicon substrate.

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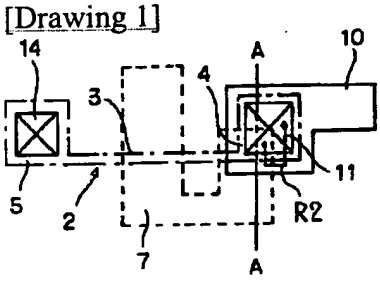
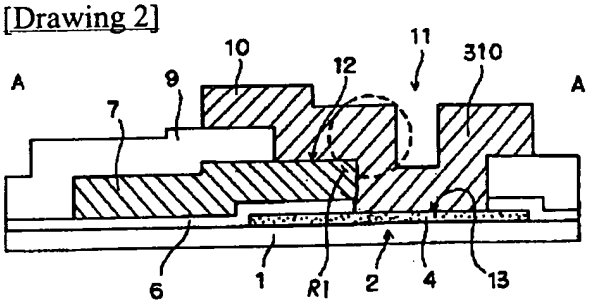
3.In the drawings, any words are not translated.

DRAWINGS

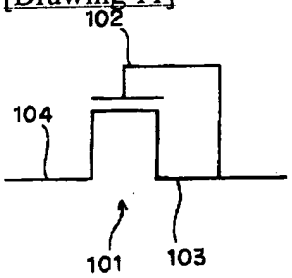
[Drawing 1]



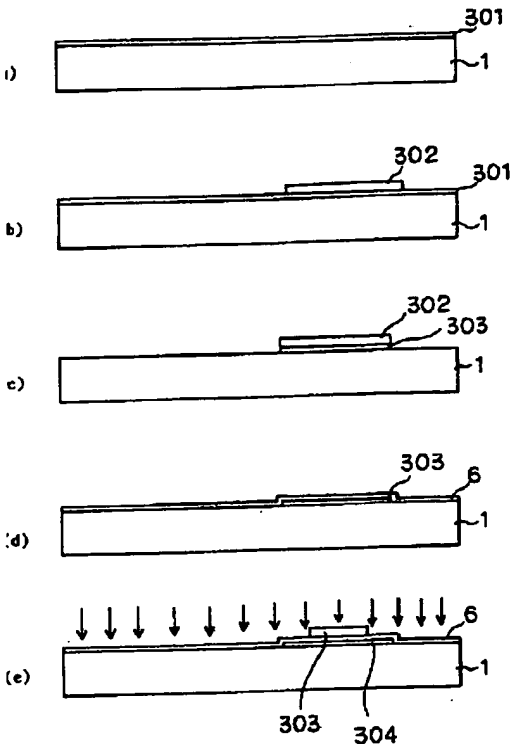
[Drawing 2]



[Drawing 11]



[Drawing 3]


301
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302
301
1
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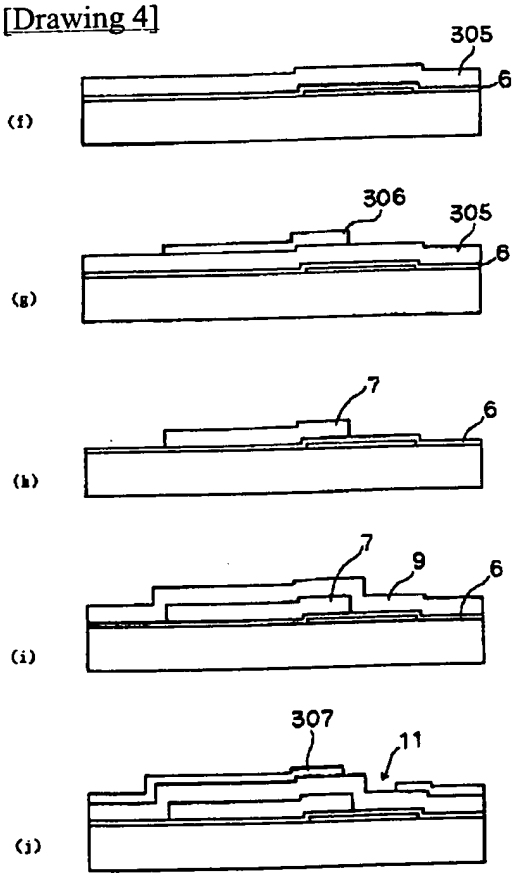
303
1
303
6
1
6
1
303
304

[Drawing 4]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306
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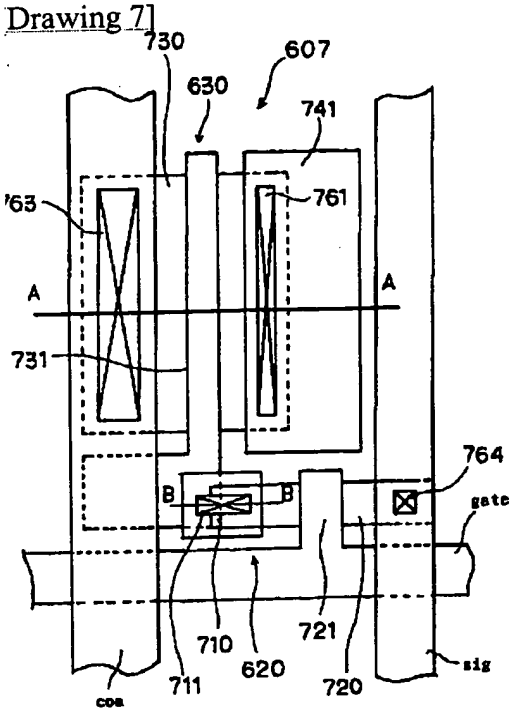
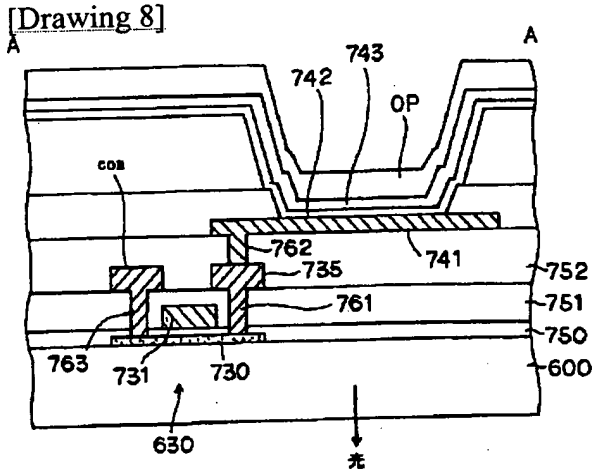
7
9
6
307
11

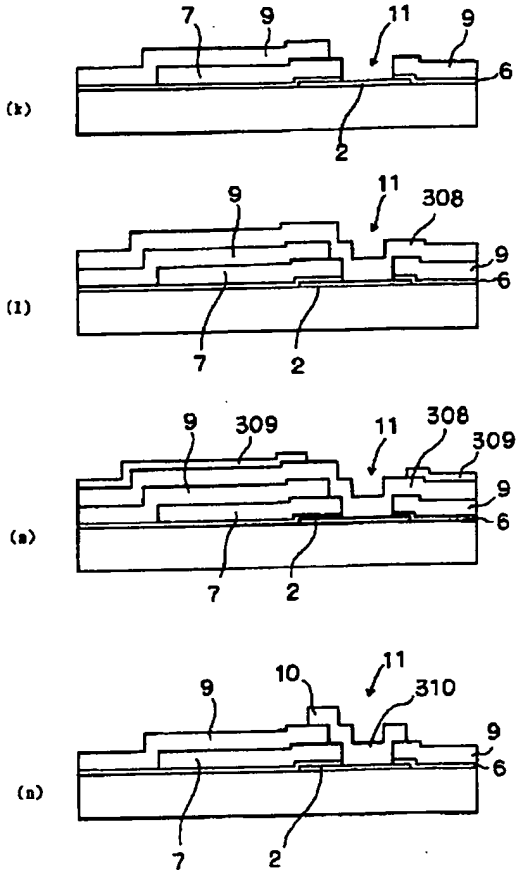
Drawing 7]



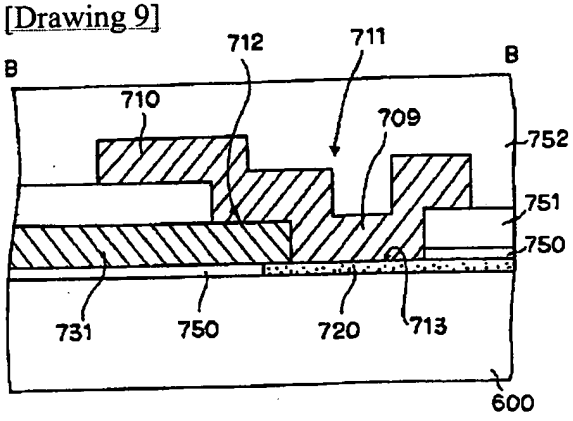
[Drawing 8]



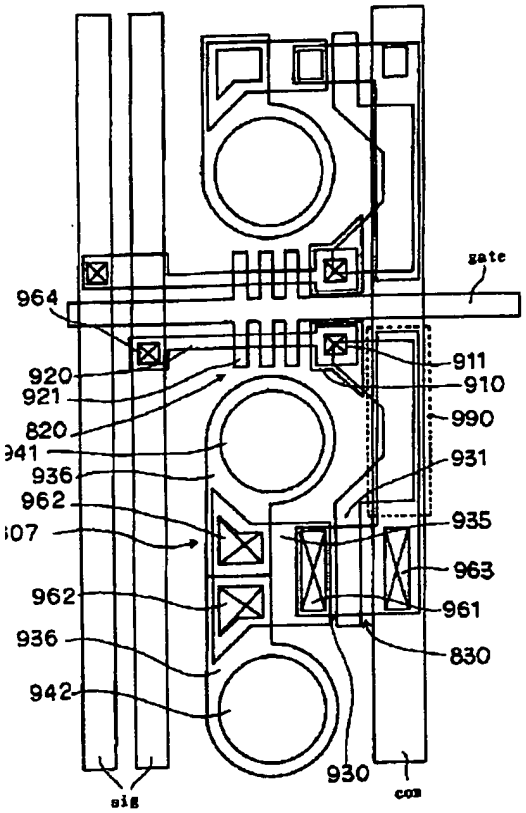
[Drawing 5]



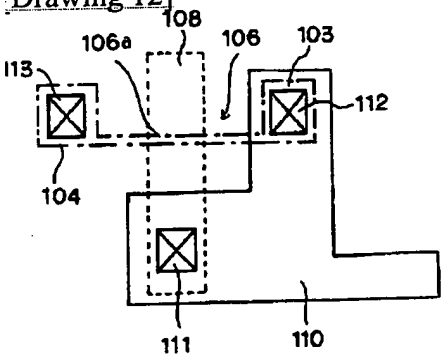
[Drawing 9]



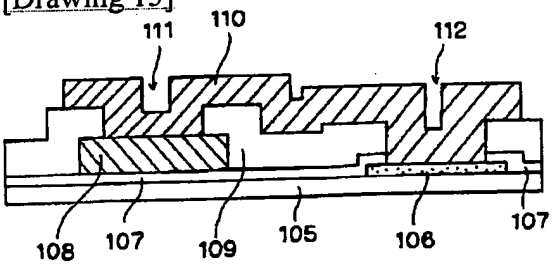
[Drawing 10]



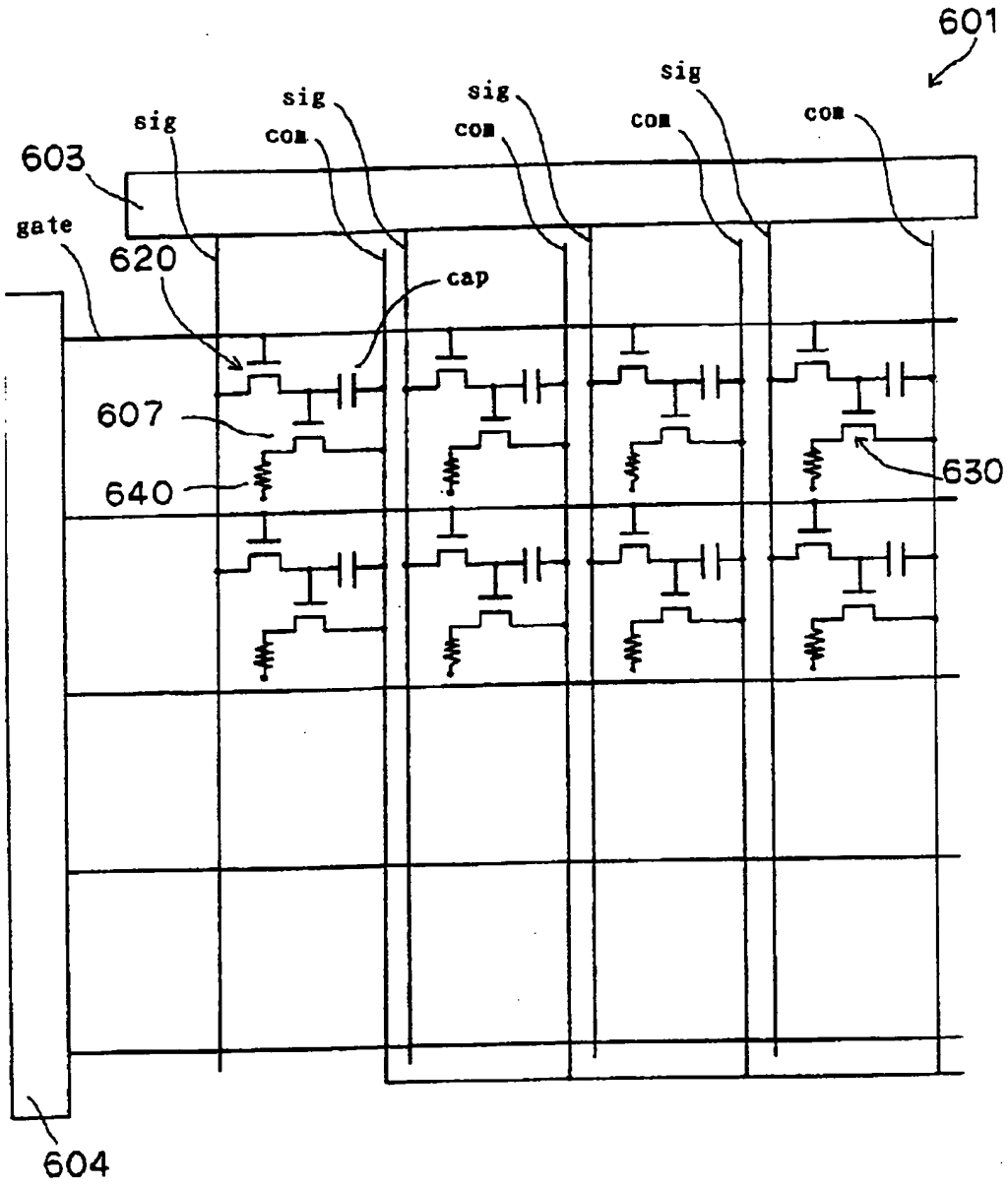
[Drawing 12]



[Drawing 13]



[Drawing 6]



[Translation done.]